Amendments to the Claims

This listing of claims will replace all prior versions and listing of claims in the application.

Listing of Claims

1. - 15. (Canceled).

16. (Previously Presented) A semiconductor device formed on a single substrate comprising:

an input and output circuit;

a memory circuit having a plurality of SRAM memory cells; and

a logic circuit;

wherein each of said plurality of SRAM memory cells has a first and second driver MISFET, a first and second transfer MISFET, and a first and second load MISFET,

wherein said input and output circuit has a plurality of first MISFETs and second MISFETs,

wherein said logic circuit has a plurality of third, fourth, fifth, and sixth MISFETs,

wherein said plurality of first MISFETs, which are n channel type, have a first threshold voltage and have gate insulating films of first thickness,

wherein said plurality of second MISFETs, which are p channel type, have a second threshold voltage and have gate insulating films of said first thickness,

wherein said plurality of third MISFETs, which are n channel type, have a third threshold voltage and have gate insulating films of second thickness, which is thinner than said first thickness,

wherein said plurality of fourth MISFETs, which are p channel type, have a fourth threshold voltage and have gate insulating films of said second thickness,

wherein said plurality of fifth MISFETs, which are n channel type, have a fifth threshold voltage and have gate insulating films of said second thickness,

wherein said plurality of sixth MISFETs, which are p channel type, have a sixth threshold voltage and have gate insulating films of said second thickness,

wherein said first threshold voltage is larger than said third threshold voltage,

wherein the absolute value of said second threshold voltage is larger than the absolute value of said fourth threshold voltage,

wherein said third threshold voltage is larger than said fifth threshold voltage,

wherein the absolute value of said fourth threshold voltage is larger than the absolute value of said sixth threshold voltage,

wherein said first and second transfer MISFETs, which are n channel type, have said fifth threshold voltage and have gate insulating films of said second thickness,

wherein said first and second load MISFETs, which are p channel type, have said fourth threshold voltage and have gate insulating films of said second thickness.

17. (Previously Presented) The semiconductor device according to claim 16,

wherein the dose of impurities in said third MISFETs are larger than the dose of impurities in said fifth MISFETs,

wherein the dose of impurities in said fourth MISFETs are larger than the dose of impurities in said sixth MISFETs,

wherein gate lengths of said third and fifth MISFETs are the same,

wherein gate lengths of said fourth and sixth MISFETs are the same.

18. (Previously Presented) The semiconductor device according to claim 17,

wherein the dose of impurities in said first and second transfer MISFETs are smaller than the dose of impurities in said third MISFETs,

wherein the dose of impurities in said first and second load MISFETs are larger than the dose of impurities in said sixth MISFETs.

19. (Previously Presented) The semiconductor device according to claim 16,

wherein said first and second driver MISFETs, which are n channel type, have said third threshold voltage and have gate insulating films of said second thickness.

20. (Previously Presented) The semiconductor device according to claim 16,

wherein said input and output circuit is placed around said memory array circuit.

21. (Previously Presented) The semiconductor device according to claim 16,

wherein the operating voltage supplied to said input and output circuit is larger than the operating voltage supplied to said logic circuit.

22. (Currently Amended) The semiconductor ~~integrated circuit~~ device according to claim 21,

wherein the operating voltage supplied to said input and output circuit is larger than the operating voltage supplied to said SRAM memory cells.

23. (Previously Presented) The semiconductor device according to claim 22,

wherein said fifth and sixth MISFETs are used for transistors comprising the critical path in said logic circuit.

24. (Previously Presented) The semiconductor device according to claim 22,

wherein said fifth and sixth MISFETs are around 10%of MISFETs in said logic circuit.

25. (Previously Presented) The semiconductor device according to claim 16,

wherein said memory circuit further comprises a peripheral circuit,

wherein said peripheral circuit has a plurality of seventh and eighth MISFETs,

wherein said plurality of seventh MISFETs, which are n channel type, have said fifth threshold voltage and have gate insulating films of said second thickness,

wherein said plurality of eighth MISFETs, which are p channel type, have said sixth threshold voltage and have gate insulating films of said second thickness.

26. (Previously Presented) The semiconductor device according to claim 25, wherein said peripheral circuit has decoder, precharge, and word driver circuits.

27. (Previously Presented) A semiconductor device formed on a single semiconductor chip comprising:

an interface circuit;

a memory circuit having a plurality of word lines, plurality of bit lines, plurality of SRAM memory cells, and a circuit for controlling said plurality of SRAM memory cells; and a logic circuit;

wherein said interface circuit has a plurality of first MISFETs and second MISFETs,

wherein said logic circuit has a plurality of third, fourth, fifth, and sixth MISFETs,

wherein each of said plurality of SRAM memory cells has a seventh, eighth, ninth, tenth, eleventh, and twelfth MISFET,

wherein the gates of said seventh and eighth MISFETs are coupled to said word lines,

wherein the gates of said ninth MISFETs are each coupled to the drains of said eleventh and twelfth MISFETs,

wherein the gates of said tenth MISFETs are each coupled to the drains of said eleventh and twelfth MISFETs,

wherein the gates of said eleventh MISFETs are each coupled to the drains of said ninth and tenth MISFETs,

wherein the gates of said twelfth MISFETs are each coupled to the drains of said ninth and tenth MISFETs,

wherein said plurality of first MISFETs, which are n channel type, have a first threshold voltage and have gate insulating films of first thickness,

wherein said plurality of second MISFETs, which are p channel type, have a second threshold voltage and have gate insulating films of said first thickness,

wherein said plurality of third MISFETs, which are n channel type, have a third threshold voltage and have gate insulating films of second thickness, which is thinner than said first thickness,

wherein said plurality of fourth MISFETs, which are p channel type, have a fourth threshold voltage and have gate insulating films of said second thickness,

wherein said plurality of fifth MISFETs, which are n channel type, have a fifth threshold voltage and have gate insulating films of said second thickness,

wherein said plurality of sixth MISFETs, which are p channel type, have a sixth threshold voltage and have gate insulating films of said second thickness,

wherein said first threshold voltage is larger than said third threshold voltage,

wherein the absolute value of said second threshold voltage is larger than the absolute value of said fourth threshold voltage,

wherein said third threshold voltage is larger than said fifth threshold voltage,

wherein the absolute value of said fourth threshold voltage is larger than the absolute value of said sixth threshold voltage, and

wherein said tenth and twelfth MISFETs, which are p channel type, have gate insulating films of said second thickness have a threshold voltage between said second and fourth threshold voltage.

28. (Previously Presented) The semiconductor device according to claim 27,

wherein said seventh and eighth MISFETs, which are n channel type, have gate insulating films of said second thickness have a threshold voltage same as said fifth threshold voltage,

wherein the dose of impurities in said third MISFETs are larger than the dose of impurities in said fifth MISFETs,

wherein the dose of impurities in said fourth MISFETs are larger than the dose of impurities in said sixth MISFETs,

wherein gate lengths of said third and fifth MISFETs are the same,

wherein gate lengths of said fourth and sixth MISFETs are the same.

29. (Previously Presented) The semiconductor device according to claim 28,

wherein the dose of impurities in said tenth and twelfth MISFETs are larger than the dose of impurities in said sixth MISFETs.

30. (Previously Presented) The semiconductor device according to claim 27, wherein the dose of impurities in said ninth and tenth MISFETs are larger than the dose of impurities in said fifth MISFETs.

31. (Previously Presented) The semiconductor device according to claim 30, wherein said interface circuit is placed around the edge of said semiconductor chip.

32. (Previously Presented) The semiconductor device according to claim 27, wherein the operating voltage supplied to said interface circuit is larger than the operating voltage supplied to said logic circuit.

33. (Currently Amended) The semiconductor ~~integrated circuit~~ device according to claim 32,

wherein the operating voltage supplied to said interface circuit is larger than the operating voltage supplied to said SRAM memory cells.

34. (Currently Amended) The semiconductor ~~integrated circuit~~ device according to claim 27,

wherein said memory circuit has a global bit line which is coupled to said plurality of bit lines through a plurality of switches;

wherein said plurality of switches each has a NMISFET and a PMISFET, which its source/drain path coupled between said global bit line and said bit line,

wherein said NMISFET has said fifth threshold voltage and has a gate insulating film of said second thickness, and

wherein said NMISFET has said sixth threshold voltage and has a gate insulating film of said second thickness.

35. (Currently Amended) The semiconductor ~~integrated circuit~~ device according to claim 27,

wherein said circuit for controlling said plurality of SRAM memory cells has a plurality of NMISFETs having said fifth threshold voltage and having gate insulating films of said second thickness, and PMISFETs having said sixth threshold voltage and having gate insulating films of said second thickness.